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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/807,307	03/24/2004	Teruhito Ohnishi	60188-817	3828

7590 11/17/2005

Jack Q. Lever, Jr.
McDERMOTT, WILL & EMERY
600 Thirteenth Street, N.W.
Washington, DC 20005-3096

EXAMINER	
NOVACEK, CHRISTY L	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 11/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/807,307	OHNISHI ET AL.	
	Examiner	Art Unit	
	Christy L. Novacek	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) *1-6* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/24/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the election filed September 14, 2005.

Election/Restrictions

Applicant's election of Group II, claims 7-11 in the reply filed on September 14, 2005 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claims 1-6 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on September 14, 2005.

Claim Objections

Claim 10 is objected to because of the following informalities:

In line 1 of claim 10, the word "having" should be replaced with "has". Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7, 8, 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohnishi et al. (US 20020158311) in view of Howard et al. (US 6,830,982).

Regarding claim 7, Ohnishi discloses epitaxially growing on a first semiconductor layer (101) of a first conductive type (n-type) surrounded by isolation layers (103), a second semiconductor layer (111b) having a different band gap from that of the first semiconductor layer and containing an impurity of a second conductivity type (p-type) so as to extend between the isolation layers, epitaxially growing on the second semiconductor layer, a third semiconductor layer (111a) having a different band gap from that of the second semiconductor layer, forming on the third semiconductor layer, an insulating film (117) having an emitter opening portion, forming on the third semiconductor layer and the insulating film, a polysilicon layer (129a/129b) containing an impurity of the first conductivity and patterning the polycrystalline layer and the insulating layer to form an emitter electrode (Fig. 2a-5b; para. 0065-0073). Ohnishi does not disclose implanting ions of an impurity of the second conductive type into the second and third semiconductor layers from a direction tilted from a perpendicular direction with respect to a surface of a substrate using the emitter electrode and the insulating film as masks. Like Ohnishi, Howard discloses a process of forming a heterojunction bipolar transistor. Howard teaches that it is advantageous to implant ions of the second conductivity type (p-type) into the third semiconductor layer (cap layer) and second semiconductor layer (extrinsic base layer) at an angle tilted from a perpendicular direction because the ions reduce the resistance of the second and third semiconductor layers (col. 5, ln. 49 – col. 6, ln. 15). Howard also discloses that this type of implant is conventional when forming a heterojunction bipolar transistor (col. 6, ln. 25-28). At the time of the invention, it would have been obvious to one of

ordinary skill in the art to use the angled implanting process taught by Howard to implant ions of the second conductivity type into the second and third semiconductor layers of Ohnishi because Howard teaches that this type of implant is conventional and offers the benefit of reducing the resistance of the cap and extrinsic base layers of the heterojunction bipolar transistor.

Regarding claim 8, Ohnishi discloses drive-in-diffusing an impurity of the first conductive type (n-type) from the emitter electrode into the third semiconductor layer to form an emitter layer in a region of the third semiconductor layer located under the emitter opening portion (para. 0027-0028). Howard does not disclose the distance from the boundary between the emitter and the second semiconductor layer and the cap layer and extrinsic base region where the ions of the second conductivity type are implanted. At the time of the invention, it would have been obvious to one of ordinary skill in the art to use routine experimentation to determine an optimal distance from the boundary between the emitter and the second semiconductor layer and the cap layer and extrinsic base region where the ions of the second conductivity type are implanted in the bipolar transistor of Ohnishi, depending upon the lengths of the intrinsic and extrinsic base regions and the desired function of the bipolar transistor because such variables of art recognized importance are subject to routine experimentation and discovery of an optimum value for such variables is obvious. See *In re Aller*, 105 USPQ 233 (CCPA 1955).

Regarding claim 10, Ohnishi discloses that the polycrystalline silicon layer has a thickness of 300 nm (para. 0072).

Regarding claim 11, Ohnishi discloses that the first semiconductor layer has a Si single crystalline composition and the second semiconductor layer has a SiGe or SiGeC mixed crystal composition (para. 0026).

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohnishi et al. (US 20020158311) and Howard et al. (US 6,830,982) as applied to claim 1 above, and further in view of Voldman (US 6,586,818).

Regarding claim 9, Ohnishi discloses forming an insulator sidewall (123) on side surfaces of the emitter electrode and the insulating film and siliciding the emitter electrode and upper portions of a silicon layer that lies on the third semiconductor layer using the insulating sidewall as a mask (para. 0074-0075). Ohnishi does not disclose siliciding upper portions of the third semiconductor layer. Like Ohnishi, Voldman discloses a process of forming a heterojunction bipolar transistor and siliciding regions of the transistor (col. 6, ln. 20-30). Voldman teaches that by exposing the extrinsic base (third semiconductor layer), the silicide can be formed directly on the extrinsic base layer, thereby advantageously reducing the resistance of the extrinsic base layer (col. 6, ln. 20-30). At the time of the invention, it would have been obvious to one of ordinary skill in the art to silicide the third semiconductor layer (extrinsic base and cap layer) of Ohnishi because Voldman teaches that siliciding the extrinsic base reduces the resistance of the base.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christy L. Novacek whose telephone number is (571) 272-1839. The examiner can normally be reached on Monday-Thursday and alternate Fridays 7:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CLN
November 14, 2005

Michael Trinh
Primary Examiner